# DAMAGE-FREE ULTRASONICALLY-ASSISTED CLEANING OF PRINTED CIRCUIT ASSEMBLIES

B. P. RICHARDS, P. BURTON and P. K. FOOTNER

*The effects of ultrasonic agitation on electronic components during PCB cleaning have long been the subject of controversy. This paper summarizes the results of a series of studies into these effects for a range of components using CFC, aqueous and semi-aqueous cleaning media. The variations with exposure time and power density under various ultrasonic stress conditions are discussed. The results are encouraging and suggest that for a large range of commonly-used components there is a large margin of safety when employing currently accepted regimes of operation and good quality components. In addition, quartz crystal devices, although more susceptible to damage than ICs, will withstand ultrasonic exposure without deleterious effects for periods several times longer than those used for cleaning PCBs, once manufacturing defects have been screened out. In the case of hybrids, the sensitivity to damage is critically dependent on the type of package used.*

*Keywords: ultrasonics; PCB cleaning; quartz crystal devices; hybrid packages.*

## 1. INTRODUCTION

In the fabrication of printed circuit boards (PCBs) it has long been recognized that effective cleaning of the boards presents a major problem, and with the implementation of surface mount technology (SMT) and more complex package types, the problem has become more significant. Moreover, this situation is now exacerbated by the current decrease in the use of CFCs resulting from the implementation of the Montreal Protocol, and the expected lower availability and increased unit costs of the CFC solvents, which for so long have been universally used as efficient cleaning and drying agents. The problem centres on the removal of contamination from essentially two locations: (1) on readily-accessible boards or tracks, and (2) that held by capillary action between component and board. Whilst the first is relatively easy to remove by a variety of means, the latter is resistant to many of these techniques. However, one of the most effective means of cleaning under components with small stand-off heights is to subject the PCB to ultrasonic agitation, a technique which is known to enhance the cleaning effects of all solvents.

Unfortunately, the use of ultrasonic agitation has, in some circles, been banned or strongly discouraged (for example, by the military), since it was considered highly likely that it would produce irreversible damage to the components themselves, and/or compromise their long-term reliability. The two major effects, to the components themselves, were expected to be breaking of the internal bond wires as a result of forced vibration, and fatigue fractures of the legs or soldered joints. These worries appear to have been based on information obtained around 20 years ago on devices, technologies and equipment (operating at 25 kHz) no longer in use; rumours and myths have been perpetuated ever since. However, until recently there has been no unambiguous information in the literature to support the view that ultrasonic agitation in state-of-the-art equipment results in device failure solely and unambiguously because of this cause. Indeed, many non-military market sectors routinely use ultrasonic cleaning with apparently no detrimental effects to either the components or the long-term reliability of the product. The agitation may well serve to highlight poor quality and incipient defects present in the components (for example, by enlarging pre-existing micro-cracks in passive components, detaching unsatisfactory bonds etc.), but does not of itself cause failure. With the use of SMT, smaller stand-off heights, larger and more complex packages, and the loss of CFCs as the mainstream solvents, the desire to use ultrasonic agitation more widely is becoming irresistible.

A programme of work(1) has therefore been undertaken with the specific aim of addressing the question: 'Does ultrasonic agitation damage modern microelectronic components?', and if so, to generate an understanding and knowledge of the processing parameters. CFC solvents were used initially because these are extensively used in the industry at the present time. However, two attractive alternatives to CFC cleaning, that is, the aqueous cleaning route and the use of semi-aqueous solvents, have also been employed. The purpose of this paper is to present the results of these investigations, and to review the effects of damage caused by the use of ultrasonic cleaning.

## 2. OBJECTIVES

The main aims of this work were:

(i) to investigate the effect of ultrasonic cleaning on a range of components using CFC, aqueous and semi-aqueous solvents,

(ii) to identify the type and nature of any physical damage induced in the chosen range of components using ultrasonic agitation,

(iii) to assess the accumulation of the damage with extended exposure time and power density, and

(iv) to define the regimes of safe ultrasonic operation consistent with adequate cleaning using the three solvent types.

With the full co-operation of the suppliers, two different ultrasonic cleaning units have been used, both operating at ~38 kHz; that is, an ICI 'Cleanline 2' operated at a mean electrical power density of about 11 W/litre, and a Kerry KS 451 tank, capable of operation over a range of power densities with a maximum of ~32 W/litre.

As the programme evolved it was apparent that the components could be categorized into those (the vast majority) that had a low sensitivity to damage from ultrasonic exposure and those which had a high sensitivity. It is convenient to consider each of these in turn.

## 3. COMPONENTS OF LOW SENSITIVITY

### 3.1. Components and Assessment Techniques

At an early stage of the investigation it became clear that many present-day components are robust and difficult to damage using ultrasonic cleaning techniques under standard exposure times and power densities (a few minutes at 10−11 W/litre). Since it was essential to distinguish between the regimes necessary to produce clean boards and those to produce device damage, these components (that is, ICs, transistors, passives, etc.) have been subjected to ultrasonic stresses (up to 32 W/litre and 100 hours) well beyond those required for cleaning, in order to map out the damage-inducing regimes. The components were stressed in three ways, as appropriate:

(i) mounted on test boards designed to accommodate a range of representative leaded and SM components (active and passive),

(ii) mounted on boards to give large numbers of the same device type, or

(iii) loose in a basket to provide maximum stress (and hence damage) on the components for a given exposure.

All the components used were from batches qualified to either MIL or commercial standards. Examinations were carried out on examples of the as-received components to ensure that the quality of the components was consistent with their purchase specification, and that any failures would not be caused by questionable quality. The component types studied and the cleaning equipment used are detailed in table 1.

**Table 1**

**Equipment and components used in damage accumulation studies**

| Component type | CFC | Aqueous | Semi-aqueous |
|---|---|---|---|
| TO-18 transistors | ✓ | ✓ | ✓ |
| DIL (ceramic, large and small) | ✓ | ✓ | – |
| DIL(plastic, large and small) | ✓ | ✓ | – |
| SOIC (Small Outline Integrated Circuit) | ✓ | ✓ | – |
| Test boards: | | | |
| PLCC (Plastic Leaded Chip Carrier); PGA (Pin Grid Array); SOIC | ✓ | ✓ | ✓ |
| DIL (plastic and ceramic) | ✓ | ✓ | ✓ |
| LED; SOT-23; diodes | ✓ | ✓ | ✓ |
| Chip resistors and capacitors | ✓ | ✓ | ✓ |
| Equipment: | | | |
| Kerry KS451 (class D driver) | ✓ | ✓ | – |
| Max. power density (W/litre) | 32 | 22 | – |
| ICI Cleanline 2 (type R2818 UV28) | ✓ | ✓ | – |
| Constant power density (W/litre) | 11 | 11 | – |
| Kerry Aquaclens | – | – | ✓ |
| Max. power density (W/litre) | – | – | 24 |

Assessment of the damage accumulation was made using essentially electrical techniques, and the nature and type of the damage and its generation were established using a range of analytical and microscopical techniques as appropriate. In order to assess the effect of ultrasonic agitation on weakening bond strengths, and hence on the possibility of compromising future field life, the strengths of a large number of bonds were measured.

## 3.2. Results – CFC Solvents

### *3.2.1. TO–18 transistors*

These devices were stressed, both soldered to circuit boards and lying loose in a wire cage, for periods of up to 100 h and power densities of up to 32 W/litre. The results clearly demonstrated that, even with high power density, long-term exposure was required in order to damage these components. For example, at normal power density exposure (11 W/litre) no damage was incurred after continuous exposure for 27 h. However, damage could be induced in shorter periods at high power densities, and fig. 1 shows the cumulative failure percentage for both mounted and loose TO–18 transistors plotted against exposure time. Further analysis of these results (2) showed that all the bonds had a mean life of 25 h with the majority surviving longer than 1000 h of normal exposure. Examination of the failed bond wires confirmed that in all cases failure had occurred, as expected, at the heel of the bond because of mechanical fatigue. The sites of the failure were at either the wire-bond pad joint (see scanning electron microscope (SEM) micrograph in fig. 2), or at the wire-terminal post joint.

### *3.2.2. Plastic DIL devices*

DIL packaged devices were stressed in a similar manner to the TO–18 transistors. Not unexpectedly, the devices proved even more robust, since the bond leads are held captive by the plastic moulding, and no bond lead failures were encountered at normal power densities for exposures up to 100 h. Some slight cavitation erosion damage to the legs on board-mounted ICs was observed for boards subjected to high power density exposure for periods in excess of 4 h (see fig. 3(a)). Under severe exposure complete breaks could be induced (see fig. 3(b)).

### *3.2.3. Ceramic DIL devices*

In ceramic packaged devices, the internal bond wires between the package legs and the silicon chip surface are free to vibrate, hence it is possible that damage could occur. Consequently, both small (4116-type 18-pin RAM and 4001-type 14-pin CMOS) and large (27C256 28-pin EPROM) packaged CMOS devices were subjected to ultrasonic agitation, and two different methods were used to assess the damage – electrical testing and bond strength measurements after de-lidding the devices.

For the smaller devices, batches of twenty-five were mounted onto boards that were then ultrasonically stressed for various periods. Electrical testing showed that whilst the 4001-type parts did not exhibit any damage after 100 h exposure (that is, no bond wire had been broken), some failures were encountered with the 4116-type parts. The subsequent bond strength distributions were then compared with similar distributions for virgin devices.

The results for the stressed 4001-type devices reflected the electrical measurements, that is, no zero gram failures, and no statistical change from the virgin bond strength distribution – see fig. 4. All the bonds are above the specification value(3) of 1.8 gm required for 30 μm diameter aluminium wires. The 4116-type memory devices, however, did incur failures for times greater than one hour (at high power densities) rising to about 10% at 100 h – see fig. 5 . It is evident that there are two (essentially straight-line) sections – the failure rate increases to ~10% after one hour, and thereafter remains essentially unaltered. Using the scaling factor of 1000 (see section 3.3) implies that no failures would be incurred after 100 h exposure at standard power densities. Figs. 6 and 7 show,

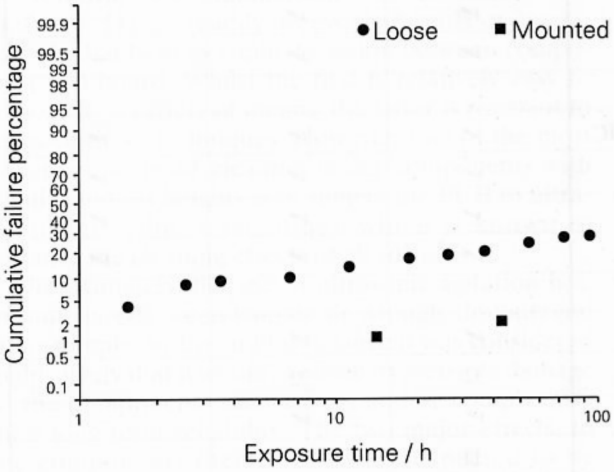

*Fig. 1. Failures of TO–can transistors at high power density in CFC*

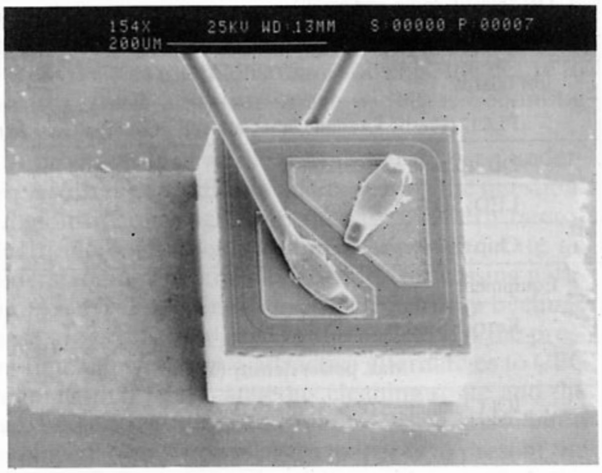

*Fig. 2. SEM micrograph showing typical fracture of wire bond after high power density exposure in CFC*

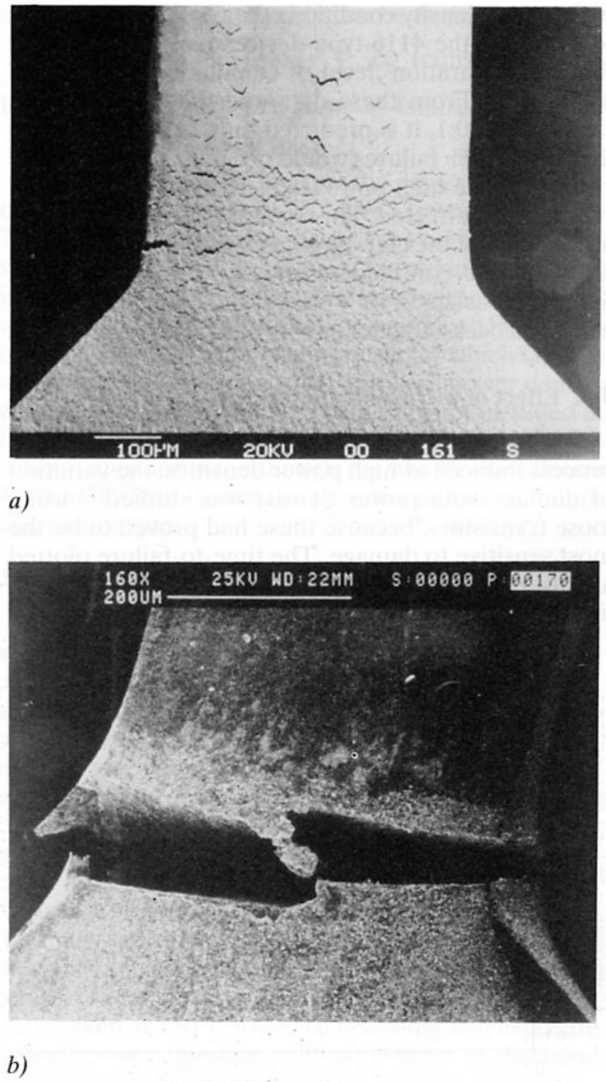

*Fig. 3. a) and b) SEM micrographs illustrating progressive fatigue damage on legs of DIP devices after high power density exposure in CFC*

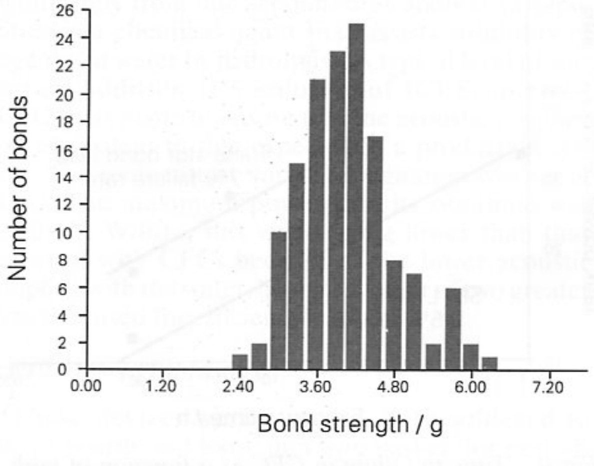

*Fig. 4. 4001-type bond strength distribution (virgin devices)*

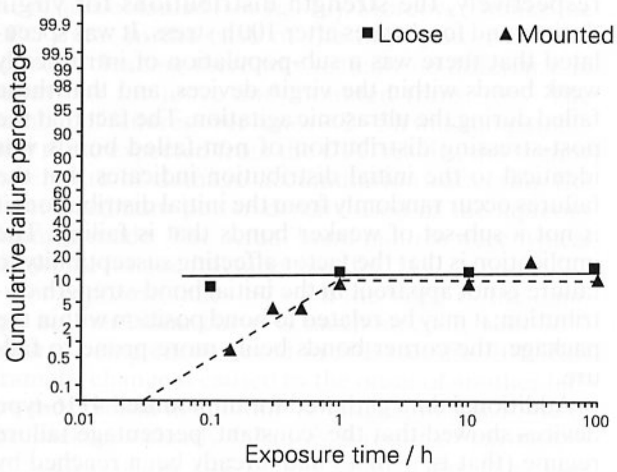

*Fig. 5. Failure of 4116-type devices at high power density in CFC*

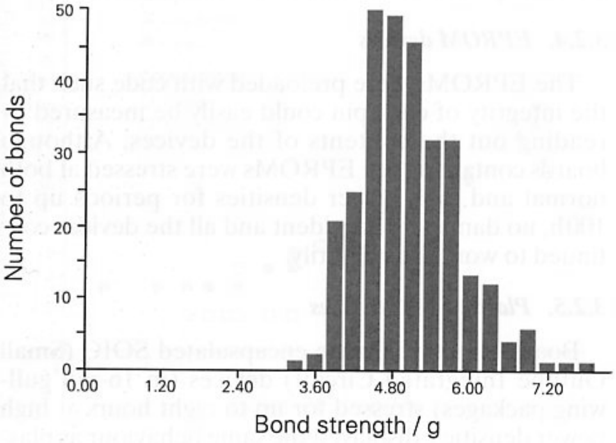

*Fig. 6. 4116-type bond strength distribution (virgin devices)*

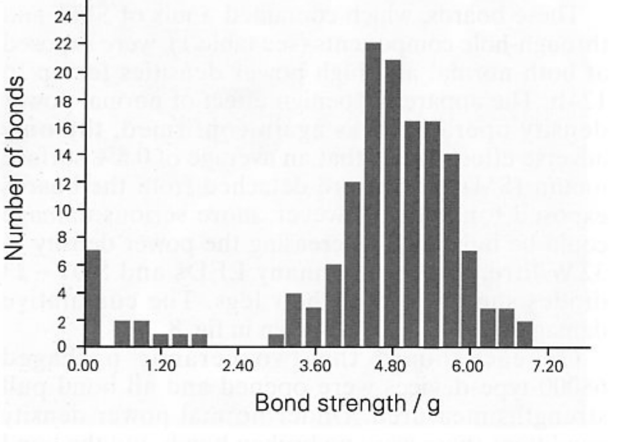

*Fig. 7. 4116-type bond strength distribution (100 h exposure in CFC; 32 W/litre)*

respectively, the strength distributions for virgin devices and for devices after 100 h stress. It was speculated that there was a sub-population of intrinsically weak bonds within the virgin devices, and that these failed during the ultrasonic agitation. The fact that the post-stressing distribution of non-failed bonds was identical to the initial distribution indicates that the failures occur randomly from the initial distribution; it is not a sub-set of weaker bonds that is failing. The implication is that the factor affecting susceptibility to failure is not apparent in the initial bond-strength distribution; it may be related to bond position within the package, the corner bonds being more prone to failure.

Additional data gathered for unmounted 4116-type devices showed that the 'constant' percentage failure regime (that is, ~10%) had already been reached by six minutes, and then continued to 100 h (see fig. 5). The fact that the 'constant' level was the same for both captive and loose devices implies that the failure mechanism was the same; in the former case the susceptible bonds were eliminated faster.

### *3.2.4. EPROM devices*

The EPROMs were preloaded with code such that the integrity of each pin could easily be measured by reading out the contents of the devices. Although boards containing ten EPROMs were stressed at both normal and high power densities for periods up to 100 h, no damage was evident and all the devices continued to work satisfactorily.

### *3.2.5. Plastic SOIC devices*

Board-mounted plastic encapsulated SOIC (Small Outline Integrated Circuit) devices (in 16-pin gull-wing packages) stressed for up to eight hours at high power densities, displayed the same behaviour as plastic DIL packages, that is, some cracking of the legs but no internal damage. However, the level of damage was much less than that experienced by the larger DIL packages, and for short times no significant damage was incurred.

### *3.2.6. Test boards*

These boards, which contained a mix of SMT and through-hole components (see table 1), were exposed at both normal and high power densities for up to 124 h. The apparently benign effect of normal power density operation was again confirmed, the only adverse effects being that an average of 0.5% surface mount (SM) LEDs were detached from the boards exposed for 124 h. However, more serious damage could be induced by increasing the power density to 32 W/litre, after which many LEDs and SOT−23 diodes sheared off at their legs. The cumulative damage for the LEDs is shown in fig. 8.

On each board the two ceramic packaged 68000-type devices were opened and all bond pull strengths measured. Under normal power density conditions there were no broken bonds and the bond strength distributions remained unaltered. Under high power density conditions the results were similar to those for the 4116-type devices (see fig. 5) except that the 'saturation' level of cumulative failures was only ~5%. From these data and the power scaling factor of 1000:1, it is predicted that, at normal power densities, 0.7% failures would occur after about 170 h.

Even at the high power density many components remained unaffected. For example, there were never any failures of the chip capacitors or chip resistors; the failures were confined essentially to the LEDs and SOT−23 packages, or to metal-lidded devices which exhibited occasional loss of hermeticity.

### **3.3. Effect of ultrasonic power density**

To gain a fuller understanding of the damage process induced at high power densities, the variation of damage with power density was studied(2) using loose transistors, because these had proved to be the most sensitive to damage. The time-to-failure plotted against power density on log−log axes gave a straight line (see fig. 9).

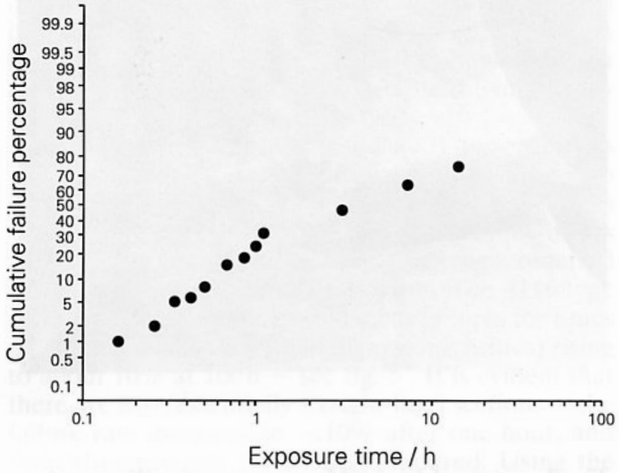

*Fig. 8. Failure of SM LEDs at high power density in CFC*

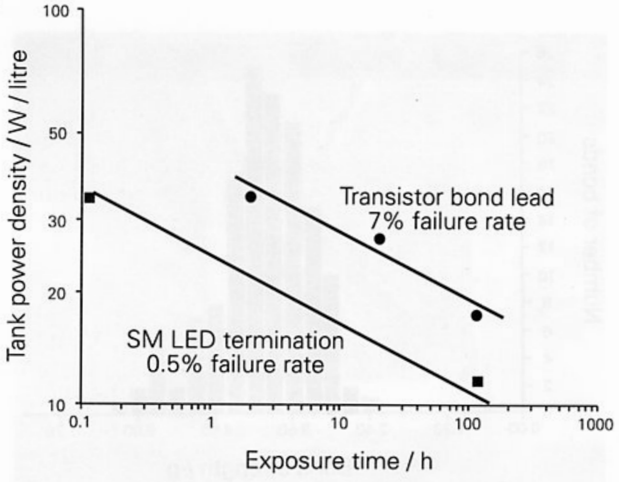

*Fig. 9. Time to failure in CFC as a function of tank power density*

The following relationship can be derived:

$$\log P = -\frac{1}{6.3}\log t + \log\ (\text{const})\,,$$

leading to the result that 'time to failure' is given by

$$t = (\text{const}) / P^{6.3}.$$

Extrapolation to 11 W/litre (the power density normally used in cleaning PCBs) gave a time of 2000 h for 7% damage compared with 2 h at the high power density used in this study. Hence, for a factor of three increase in power density, the time required to accumulate the same level of damage is reduced by a factor of 1 000. The only other components for which failures were obtained at both normal and high power density were the SM LEDs. The relevant data are included in fig. 9 and indicate that the acceleration factor of 1 000 is again appropriate, although the two types of device were radically different, as were the modes of failure and failure rate.

### 3.4. Accelerated testing

In order to explore the possibility that ultrasonic agitation could give rise to incipient damage with consequential degradation of field performance, accelerated tests have been carried out. There are two broad categories of accelerated tests: those based on a thermal stress and those which give rise to a mechanical stress. Because the exposure to ultrasonic agitation gives rise to mechanical effects, further mechanical stress would only continue the same process, and generate no new information. Hence, although it was considered unlikely that any thermally-activated failure processes were involved, a thermal exposure stress exercise was undertaken for completeness. A group of the 4116-type RAM devices were baked at 150°C for 124 h following 10 h exposure at high power densities, but no change in the bond wire strength distribution was observed at any stage.

### 3.5. Results – aqueous solvents

Only one saponifier was used since it was believed(4) that any variations in the acoustic coupling of the water by the addition of a saponifier would not vary significantly from one saponifier to another (a saponifier is a chemical agent that assists solubility of organics in water by hydrolysis). A typical level of surfactant addition (1% solution of ICI Synperonic NP-12) was made to ensure that the acoustic coupling was equivalent to that expected in a production system. The temperature for water agitation was set at 70°C. The maximum power density obtained was ~ 20–22 W/litre, this value being lower than that achieved with CFCs because of the lower acoustic coupling with the water, but still a factor of two greater than that used for efficient cleaning.

#### *3.5.1. TO–18 transistors*

These devices were stressed, both soldered to circuit boards and loose in a wire basket, for periods up to 100 h. The board-mounted transistors were agitated whilst being suspended from wires or held rigidly, but no significant differences were noted in the results obtained (see fig. 10). Moreover, unlike the CFC data, in the case of the high power density aqueous cleaning there was virtually no difference in behaviour for loose and mounted transistors. The number of failures over times <2–5 h was comparable with those expected from the CFC results, the slightly lower rate of damage accumulation reflecting the lower maximum power density used in the aqueous cleaning mode. The actual bond failures were typical ultrasonic fatigue fractures (see fig. 11).

For exposure times >2–5 h the slope of the damage accumulation curve is much steeper, with 70% failures being encountered in 50 h (see fig. 10). This dramatic change is caused by the onset of another failure mechanism in addition to fatigue, that is, some of the packages clearly failed as a result of cavitation-induced erosion and penetration of the can. This change in the dominant failure mechanism can be

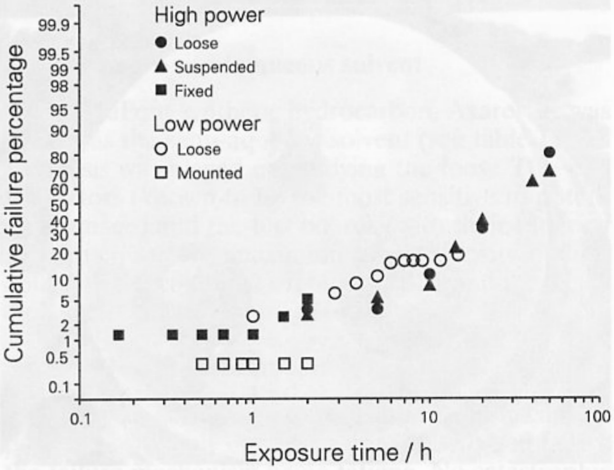

*Fig. 10. Cumulative failures as a function of exposure time in an aqueous solvent for mounted and loose TO–can transistors*

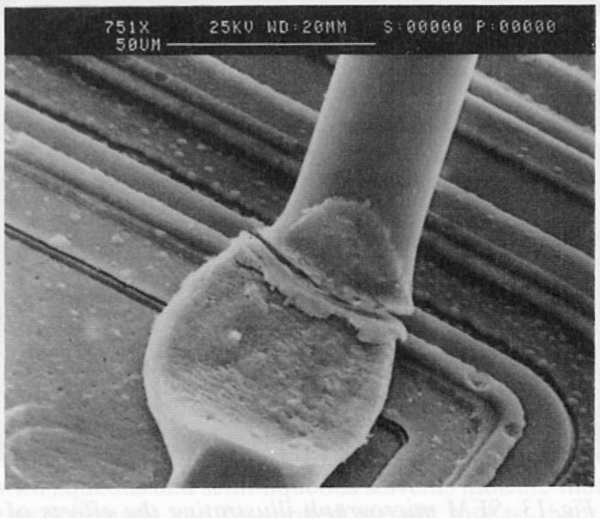

*Fig. 11. SEM micrograph illustrating typical ultrasonic bond fatigue failure using aqueous solvent*

explained(4) in terms of corrosion accelerated by ultrasonic breakdown of the normal 'passivating' boundary layer, and final penetration of the can and water ingress (see fig. 12).

Clearly such puncturing of the package (see fig. 13) is undesirable, but it must be emphasised that it occurs only in times that are still at least two orders of magnitude longer than those required for efficient cleaning. Moreover, this process cannot be extrapolated back to short times in order to derive, say, the p.p.m. failures in a few minutes. The chemical nature of the corrosion will require a finite time to penetrate the package, determined by the thinnest part of the package wall.

### *3.5.2. DIL devices*

Boards containing twenty plastic DIL 74LS47 devices were exposed to the higher power density for up to 40 h. In common with the CFC data there was no internal damage observed, and the external damage to the IC legs encountered after a few hours' CFC ultrasonic exposure, was not present even after 40 h exposure. In some cases the plating on the legs exhibited signs of erosion, but no cracks formed in the underlying metal. This difference of behaviour is thought to reflect the difference in maximum power densities achieved in the two solvents.

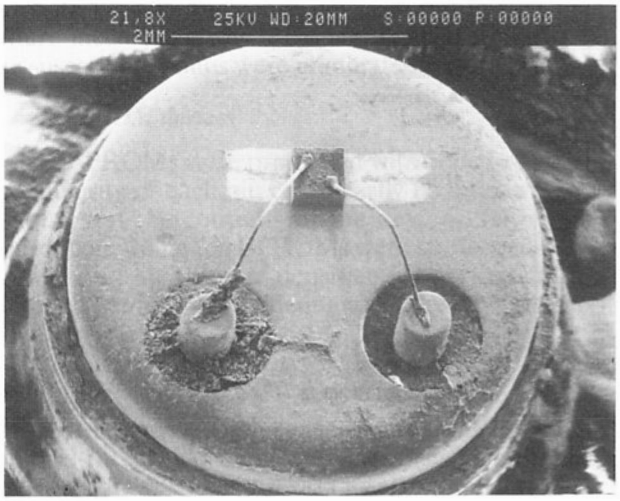

*Fig. 12. SEM micrograph illustrating corrosion of the bond wire following water ingress of the TO−can*

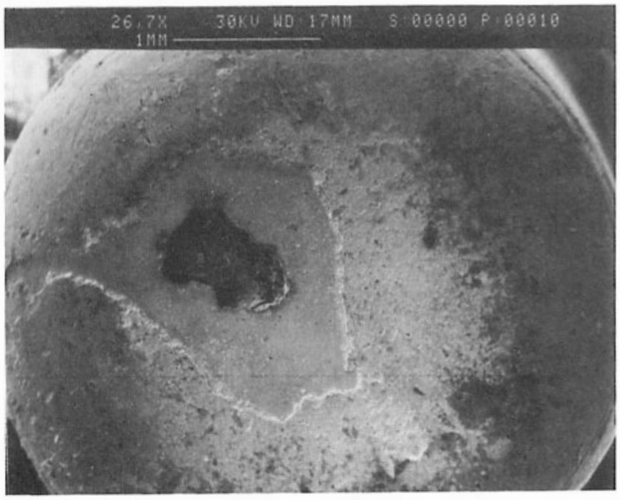

*Fig. 13. SEM micrograph illustrating the effects of cavitation and cavitation-enhanced corrosion of TO−can in an aqueous solvent*

In the case of the ceramic DIL devices of more recent technology (4001-type CMOS parts), there were no failures, a situation mirroring that obtained with the CFC medium. The level of failures incurred for the older 4116-type RAM parts (only one bond failed, 0.3% failures, after 100 h) was a factor of 20−30 down on that observed using CFC solvents, and this is again believed to reflect the difference in maximum power densities used.

### *3.5.2. Plastic SOIC devices*

Since the CFC results had indicated that only a low level of damage to device legs might be expected, only four exposure times (20, 40, 80 and 100 h) and the higher power density were used. Again the results showed that it is very difficult to damage SOIC legs using ultrasonically-enhanced water cleaning. No cracks were observed, although one leg was broken after 100 h. Unexpectedly, another (non-device) failure mechanism became operative during this exercise. The solder on some joints became increasingly cavitation-eroded with time, and in a few instances was completely removed after 100 h. This would clearly allow greater movement of the leg under ultrasonic agitation than would otherwise occur. Indeed, the broken leg observed had been completely detached from the board, presumably via this process.

### *3.5.3. Test boards*

The effects of ultrasonic agitation of the test boards in water were, as observed for the component types, less marked than for the equivalent exposure to CFCs. For example, the LEDs did not become detached from the board. The extent of damage accumulation for various component types is illustrated in fig. 14, and it is evident that even for the most sensitive devices (the LEDs) there were only 30% failures after 100 hours continuous exposure.

The majority of the damage observed was more related to cavitation erosion than to cracking. In the case of the LEDs, the clear plastic resin encapsulating the light emitting diode exhibited erosion. Initially after 10 h, the erosion was in narrow areas producing narrow fissures, but subsequently, large pieces broke away, followed in some cases by complete removal and loss of the internal bond wires (see figs. 15 and 16). Other components also became partially detached, because of the failure of the solder joint by cavitation erosion, the signs of which became visible after 20−30 min and progressively increased with time. A rather severe case of solder erosion on a chip capacitor is shown in fig. 17.

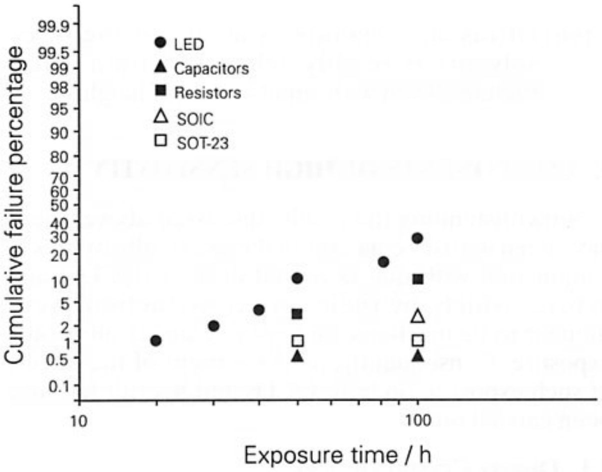

*Fig. 14. Cumulative failures as a function of exposure time at high power densities for SM components using aqueous solvents*

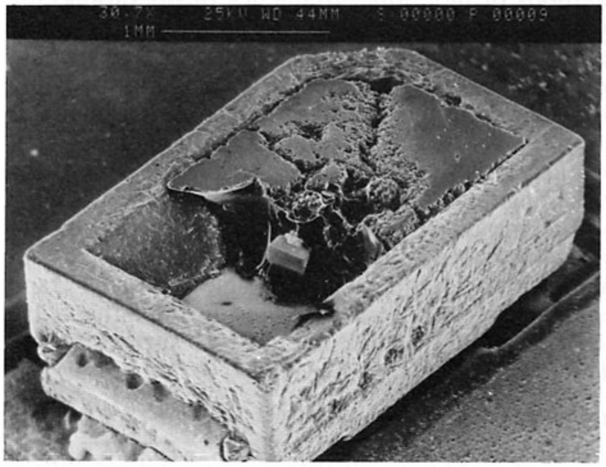

*Fig. 15. SEM micrograph illustrating the early stages of removal of the plastic from an LED as a result of cavitation in aqueous solvents*

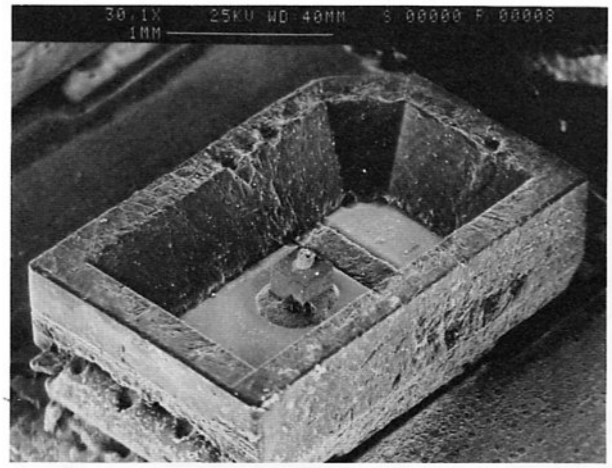

*Fig. 16. SEM micrograph showing complete removal of the plastic and bond wire from an LED as a result of cavitation in aqueous solvents*

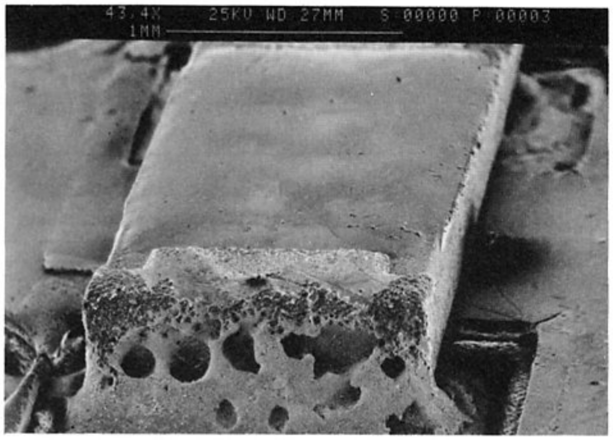

*Fig. 17. SEM micrograph illustrating cavitation erosion of solder of an SM component in an aqueous solvent*

### 3.6. Results – semi-aqueous solvent

The DuPont synthetic hydrocarbon, Axarel 38, was chosen as the semi-aqueous solvent (see table 1) and emphasis was placed on studying the loose TO–can transistors (known to be the most sensitive to potential damage) and the test boards (with their range of components). The maximum power density obtainable with the combination of Axarel 38 and the Kerry Aquaclens equipment was 24 W/litre.

#### *3.6.1. TO–can transistors*

After 95 h accumulated exposure at the maximum power density only one transistor (of 200) had failed, the failure mechanism being fatigue. No catastrophic cavitation-related damage was encountered, reflecting the difficulty of producing cavitation in the semi-aqueous medium as compared with aqueous solvents.

#### *3.6.2. Test boards*

In common with the aqueous-tested boards no components became detached from any of the three boards even after 95 h exposure, and all the components continued to function correctly. However, the plastic encapsulant of some of the LEDs did exhibit the early signs of crazing. This effect was not observed after 50 h exposure.

### 3.7. Discussion of low sensitivity components

The results for these 'low sensitivity' devices are very encouraging for users of PCBs, in that, if ultrasonic agitation is employed in conjunction with CFC, aqueous or semi-aqueous solvents, there is a large margin of safety before any damage to the components is incurred. This safety margin for CFCs is shown schematically in fig. 18, but the results obtained with aqueous and semi-aqueous solvents indicate that this schematic can be applied equally well to them. Although the results presented relate strictly to only the range of components studied, recent US data(5)

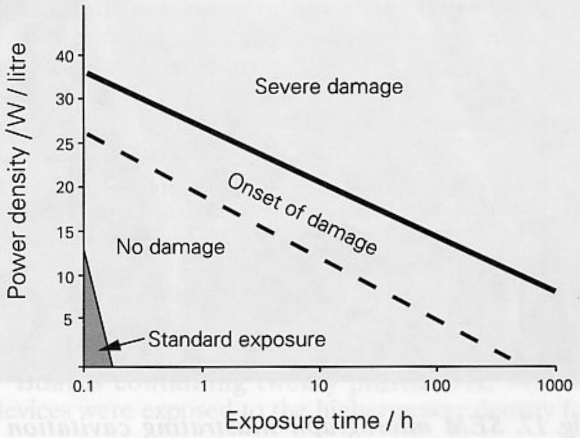

*Fig. 18. Zones of damage and CFC cleaning regimes*

obtained on other components (selected on the basis of their perceived sensitivity to resonance effects) suggest that the benign nature of the ultrasonic agitation is of more general applicability.

Salient points from these studies of 'low sensitivity' devices are as follows.

(i) Using currently accepted regimes of ultrasonic cleaning of PCBs (that is, a few minutes at ~ 11 W/litre in CFC, aqueous or semi-aqueous solvents) no damage has been encountered with **the range of components studied.**

(ii) Using abnormally high power densities (~ 30 W/litre with CFCs, 20–24 W/litre with aqueous or semi-aqueous solvents), damage can be induced in some components, but only after at least 10 min ultrasonic exposure.

(iii) Using abnormally long ultrasonic exposure times (that is, about 100 h at standard power densities), damage can be induced in some components.

(iv) The power density/time relationship is such that, for an increase in the power density of a factor of three, the time required to accumulate the same level of damage is reduced by a factor of 1000. Thus there is a need to specify and tightly control the power density used (see section 3.3).

(v) In all cases in which damage has been induced using CFC solvents, it is of a purely mechanical nature caused by fatigue, and is located on the device bond-wires and/or package legs.

(vi) Fatigue damage incurred using aqueous and semi-aqueous solvents was generally less than that using CFCs. However, an additional failure mechanism (that is, cavitation-erosion and cavitation-enhanced corrosion) was encountered with aqueous solvents after a few hours' exposure at high power density.

(vii) Ultrasonic cleaning using any of the three solvents is readily achieved within a few minutes, even with small stand-off heights.

## 4. COMPONENTS OF HIGH SENSITIVITY

Notwithstanding the results discussed above, there have been worries concerning the use of ultrasonics in conjunction with quartz crystal devices (QCDs) and hybrids which, by their very construction, were thought to be mechanically unstable under ultrasonic exposure. Consequently, an assessment of the effects of such exposure on both QCDs and hybrids has also been carried out.

### 4.1. Quartz Crystal Devices

A specially designed board (see fig. 19) which accommodated 7 devices (6 resonators and an oscillator) was used, in which the components were chosen to provide a range of package styles, crystal sizes, methods of mounting, frequency of operation etc., typical of the products used in the industry – see table 2. Products containing high cost devices would not normally be subjected to processing involving ultrasonics, but this type of QCD has been used in this study to provide a more complete picture of any damage accumulation. The test boards were stressed by mounting them rigidly in a small rack which was hung within the ultrasonic tank, and a summary of the boards examined, the exposures given, and the examination intervals is presented in table 3. Both CFC and aqueous solvents were used, and in the latter a 1% solution of ICI Synperonic NP–12 surfactant was added.

#### *4.1.1. Possible failure modes*

It was expected that two types of 'failure' might occur to the QCDs, *viz.* an alteration in the electrical parameters, and/or catastrophic breakage of either the quartz slice itself or its mount. In consequence, the test board was designed to be compatible with automatic monitoring equipment available for the precision measurement and evaluation of crystal resonators. Any changes in electrical parameters

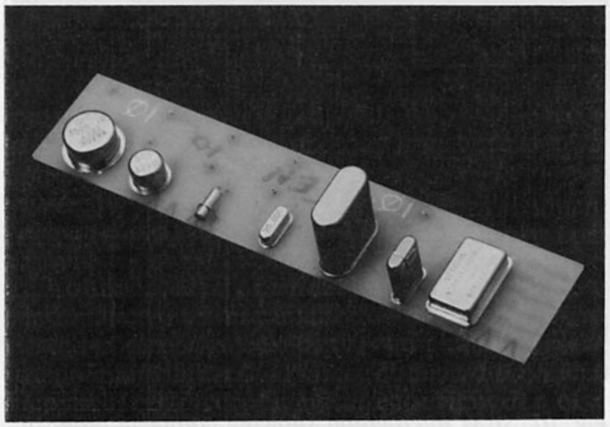

*Fig. 19. Photograph of test board and quartz crystal units*

**Table 2**
**Description of quartz crystal devices used on test boards**

| Type | Operating frequency | Package | Description |
|---|---|---|---|
| Oscillator | 32 MHz | DIL | Circular crystal held horizontally using a 3-pt fixing and silver-loaded epoxy to provide a high shock resistance mounting |
| A. Resonator | 8.192 MHz | HC49/J | Circular crystal held vertically in slotted Ni tapes using silver-loaded epoxy; silver electrodes |
| B. Resonator | 1.256 MHz | HC33 | As A; gold electrodes |
| C. Resonator | 20 MHz | HC49/5H | Typical of low cost product used in microprocessors; manufactured automatically in large volume. Rectangular crystal held horizontally using a 2-pt fixing and silver-loaded epoxy; silver electrodes |
| D. Resonator | 32.767 kHz | 3 x 8 mm cylindrical | Typical of low-cost product used in watches; manufactured automatically in large volume. The 'tuning fork' is mounted vertically using a Sn-Pb alloy; silver electrodes |
| E. Resonator | 20 MHz (third overtone) | HC35/U (TO5) | High quality precision resonator using highly polished miniature plano-convex crystal; gold electrodes |
| F. Resonator | 12 MHz | HC37/U (TO8) | High quality precision resonator using highly polished crystal; gold electrodes |

**Table 3**
**Details of the QCD test boards, exposures and examination intervals**

| Solvent | Power density (W/litre) | Exposure time (min) | No. of boards | Board numbers | Examination intervals (min) |
|---|---|---|---|---|---|
| CFC | 11 | 10 | 5 | 3−7 | 0, 1, 2, 3, 5, 10 |
|  | 11 | 60 | 1 | 2 | 5, 10, 20, 30, 40, 50, 60 |
|  | 30 | 10 | 4 | 17−20 | 0, 1, 2, 3, 5, 10 |
|  | 30 | 480 | 1 | 1 | 0, 60, 120, 180, 240, 300, 480 |
| Aqueous | 24 | 3 | 4 | 13−16 | 0, 1, 2, 3 |

could thus be readily recorded. In all cases four main features have been monitored:

(a) *Complete catastrophic failure*. In these cases the packages were opened and the failure mode identified using standard failure analysis techniques.

(b) *Any changes in $R_m$, the inherent resistance in the electrical path to the electrodes*. Historical experience(6) of changes in $R_m$ for both low-cost, high-volume and high-cost, low-volume products were used to evaluate potential problems during life. The manner in which any changes occurred in $R_m$ is also an indication of the likely failure mode. For example, a steady increase in $R_m$ is probably associated with coalescence and/or propagation of microcracks in the mounting medium. Sudden increases in $R_m$ can be attributed to larger cracks suddenly appearing, and constant (but non-increasing) high values to the presence of non-propagating cracks. Finally, any erratic behaviour is probably associated with a relatively 'loose-fit' of the crystal in its mounting, possibly following cracking of the mounting medium.

(c) *The resonant frequency*. As far as the vast majority of users is concerned this is the parameter of prime importance, and small changes in $R_m$ are of little significance. However, in the majority of the results obtained, the frequency exhibited little, if any, change from its initial time zero value (changes were <1 p.p.m.).

(d) *Q factor*. This quality parameter has a strong dependence on $R_m$.

In view of (c) and (d), it was decided that, in the assessment of results, emphasis would be placed on (a) and (b). In the case of the oscillators, a simple measurement was made of the frequency and the associated waveform, with any changes from the time zero values being noted.

### *4.1.2. Results*

As might have been anticipated, the results of this limited survey indicated(6) that QCDs are much more sensitive to ultrasonic agitation than ICs or passive components. However, although there was a range of behaviour exhibited by the chosen devices, the performance of most of them was very encouraging. The results fell into two groups, those representing (a) low-cost, high-volume devices which would be the most likely to be subjected to ultrasonic agitation during PCB assembly/processing, and (b) high-cost, low-volume types of device which, because of their intended applications, would be unlikely ever to experience ultrasonic agitation.

### *4.1.3. Low-cost, high-volume quartz crystal devices*

In the majority of applications for this type of device, any drifts in $R_m$ are of little consequence, and of prime importance is whether or not the device fails completely. Bearing this in mind, the results for this type of device were especially encouraging (see table 4) and suggested that once 'infant mortalities' (that is, failures in under two minutes' exposure) have been screened out, they will survive ultrasonic agitation (at either normal or high power densities) for lengths of time well in excess of those required for efficient PCB cleaning. The fact that infant mortalities were encountered suggests that manufacturing defects were present, but this is not surprising in view of the very low cost of such devices. Indeed, the time zero failures reflect the proportions of poor quality in these low cost devices. Clearly, ultrasonic agitation can be used as a screen for such defects.

### *4.1.4. High-cost, low-volume quartz crystal devices*

The performance of this category (fabricated for very high reliability) was markedly different from that for the low cost, 'dispensable' counterpart. There were no infant mortalities or time zero failures, reflecting both the stringent manufacturing processes and extensive testing for this type of device. Moreover, catastrophic failures occurred only after extended ultrasonic exposure times (see table 4), a feature associated with the enhanced quality of this type of component. The devices also appeared to be more subject to changes in $R_m$, reflecting the differences in crystal mounting.

### *4.1.5. Modes of failure*

There appeared to be two failure mechanisms:

(i) Breaking of the crystal (along crystallographic axes – see fig. 20) where the style/geometry of the mounting provided little or no compliance. The oscillator was typical of this category.

(ii) Breaking of the mounting medium where the style/geometry of the mounting did provide a degree of compliance. In this category, failure was via fatigue of either the mounting medium itself (for example, silver-loaded epoxy) or of the metal support. The former was operative in the low-cost, high-volume devices in which the mounting is designed to be compliant to withstand the stresses likely to be experienced. The initial fatigue quickly leads to micro-cracking (with associated increases in $R_m$) and eventual separation (see fig. 21) and device failure. The latter (only one case – see fig. 22) was operative in a high-cost, high-reliability device which would not be expected to be subject to the same levels of stress.

**Table 4**

**Summary of results of damage to quartz crystal devices**

| **Low-cost, high-volume product** | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Test vehicle** | **A** | | **B** | | **C** | | **D** | | **Totals** | |
| | **Full failures** | $R_m$ | **Full failures** | $R_m$ | **Full failures** | $R_m$ | **Full failures** | $R_m$ | **Full failures** | $R_m$ |
| CFC normal PD | 1/6 | 2/6 | 0/6 | 1/6 | 1/6 | 0/6 | 0/6 | – | 2/24 | 3/18 |
| CFC high PD | 0/5 | 1/5 | 0/5 | 0/5 | 1/5 | 0/5 | 0/5 | – | 1/20 | 1/15 |
| Aqueous high PD | 0/4 | 1/4 | 1/4 | 1/4 | 0/4 | 0/4 | 0/4 | – | 1/16 | 2/12 |

| **High-cost, low-volume product** | | | | | | |
|---|---|---|---|---|---|---|
| | **E** | | **F** | | **Totals** | |
| | **Full failures** | $R_m$ | **Full failures** | $R_m$ | **Full failures** | $R_m$ |
| CFC normal PD | 1/6 | 0/6 | 0/6 | 1/6 | 1/12 | 1/12 |
| CFC high PD | 1/5 | 1/5 | 1/5 | 1/5 | 2/10 | 2/10 |
| Aqueous high PD | 0/4 | 1/4 | 0/4 | 2/4 | 0/8 | 3/8 |

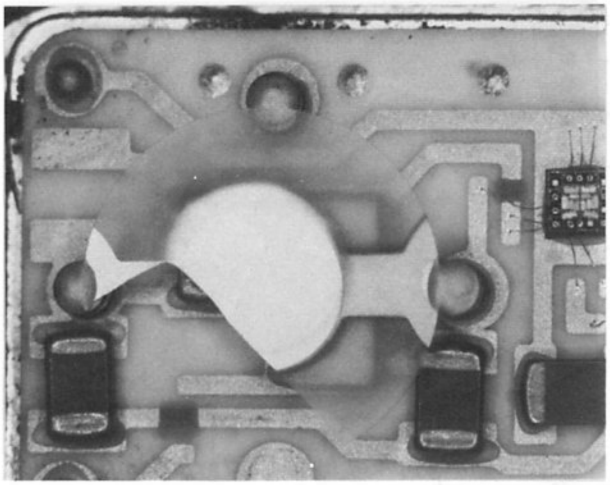

*Fig. 20. SEM micrograph of a broken crystal in an oscillator device exposed at high power density in CFC*

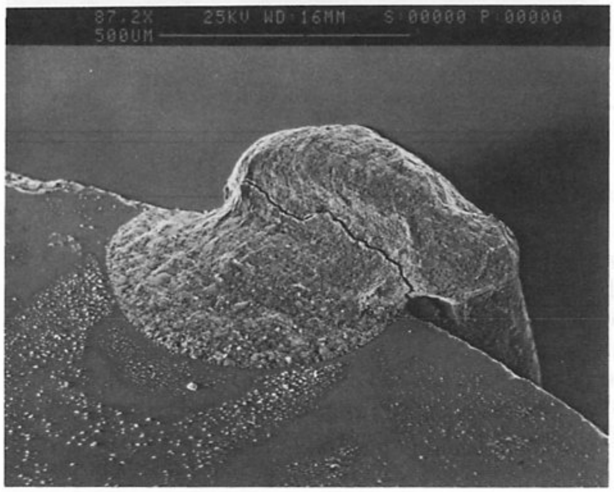

*Fig. 21. SEM micrograph of cracked support medium of a quartz crystal resonator exposed at high power density on CFC*

### *4.1.6. Discussion of quartz crystal devices*

In common with the results on ICs and transistors, these findings are encouraging and indicate that ultrasonically-assisted cleaning of PCBs is not necessarily detrimental to the performance of QCDs, but the margin of safety is not as large as that for ICs and passive components. Salient points were as follows:

(i) QCDs are more susceptible to damage from ultrasonic agitation than ICs or passive components. Hence, ultrasonic cleaning of boards containing such devices can be undertaken, but with some reserve.

(ii) Certain QCDs are more susceptible than others, largely because of the method of mounting the crystals.

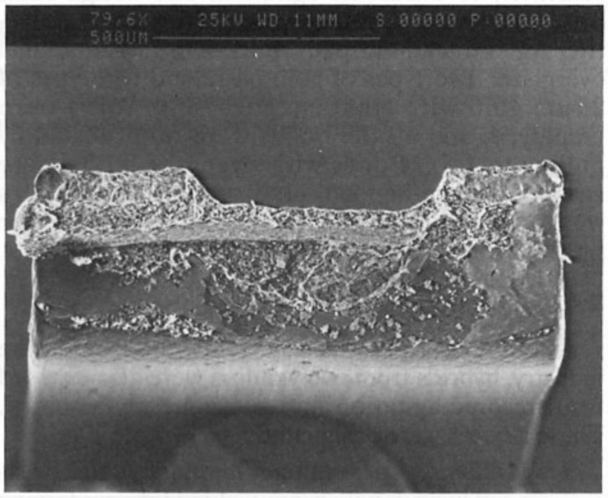

*Fig. 22. SEM micrograph of fatigue failure of support medium of a resonator exposed at high power density in CFC*

(iii) Certain QCDs contain manufacturing defects which can be screened out as infant mortalities using ultrasonic agitation as the screen.

(iv) Many QCDs (including screened products) will withstand ultrasonic exposure without any deleterious effects for periods that are several times greater than those usually used for cleaning PCBs.

## 4.2. Hybrids

The feedback gathered on field experience of hybrid devices presented a confusing picture. Some users had encountered no problems after having successfully used ultrasonic cleaning techniques on their product for several years. Others reported failures after only a few seconds of ultrasonic agitation, and subsequent analyses of the broken bonds clearly confirmed fatigue as the failure mode. This exercise was therefore aimed at addressing this apparent dichotomy.

In the construction of hybrids there are several aspects which differ from those of conventional PCBs and ICs: longer bond wires are used, the substrate materials and methods of die-attach are different (which may affect acoustic coupling), and other technologies (for example, thick film) are employed. Hence, the overall philosophy was that of a short exercise to ascertain the effect of these factors on hybrids based on ceramic substrates, using both test vehicles and commercial products.

### *4.2.1. Test vehicles*

A test vehicle was designed$^{(7)}$ to take into account as many as possible of the materials and construction features (for example, choice of pastes for tracks, firing schedules, bonding conditions and subsequent thermal treatments for sealing etc.) on those hybrids which, from field data, had exhibited a very high sensitivity to ultrasonic agitation. The design comprised six layers: first dielectric, gold, second dielectric, Ag–Pd lead-out pads, thick-film resistors, final overglaze. Two types of gold paste and two types of 25 μm gold wire (that is, 'hard' and 'soft') were employed, and all the bonds were proof-tested by pulling to 1.5 g. Bonds with strengths <1.5 g were stripped and re-bonded, after which the substrates were lidded using a metal cap and an epoxy glue (see fig. 23).

### 4.2.2. *Commercial product*

As examples of products currently used within the industry, hybrids from two vendors were also exposed to ultrasonic agitation and subsequently assessed. These devices were designated:

- *Vendor A.* Conventional hermetic metal packaged hybrids with seam-welded lids, containing an alumina substrate bonded to the base of the package using epoxy resin (see fig. 24). Internal gold wire leads connected the metal tracks to the appropriate pins of standard glass-metal seals.
- *Vendor B.* Hybrids of a simpler construction consisting of alumina substrates with legs soldered to the periphery of the tile (see fig. 25). Protection of the internal circuitry was afforded by an alumina lid epoxied over the substrate. Internal gold leads connected the metal tracks to the leadout legs.

### 4.2.3. *Assessment procedure*

In this study, only a CFC solvent (Arklone AM) was used, since the earlier results clearly indicated that the damage was not significantly different when CFC, aqueous, or semi-aqueous solvents were used. Although the hybrids were initially exposed to both high and low power density agitation, the results were such that, for the majority of the exercise, only low power density (that is, that normally used in production) was used. Every hybrid (test vehicle or commercial device) was stressed by holding it individually in a small copper gauze cage hanging in the ultrasonic tank. Up to five cages were exposed simultaneously, and a summary of the hybrids examined, the exposures given, and the examination intervals is given in table 5.

It was expected that any 'failures' occurring in the test vehicles would involve degradation and eventual breakage of the internal wire bonds. Indeed, this feature was central to the design of these vehicles. Other potential damage (for example, to legs or package cans) was believed to be secondary to bond wire failure, and hence was not taken into account in the test vehicle design. Any such mechanisms, if operative, would become manifest in the commercial product. There were five main stages in the assessment of the hybrids:

(i) Measurement (after pre-determined intervals – see table 5) of the resistance of each chain within the unopened test vehicle, an open circuit indicating that one or more of the 18 bonds within a chain had failed (note that there were four chains per test piece). No change to the time-zero value indicated that no damage

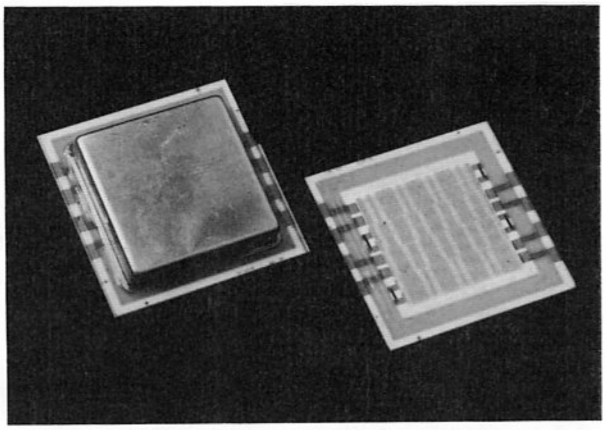

*Fig. 23. Photograph of hybrid test vehicle (as bonded and as capped)*

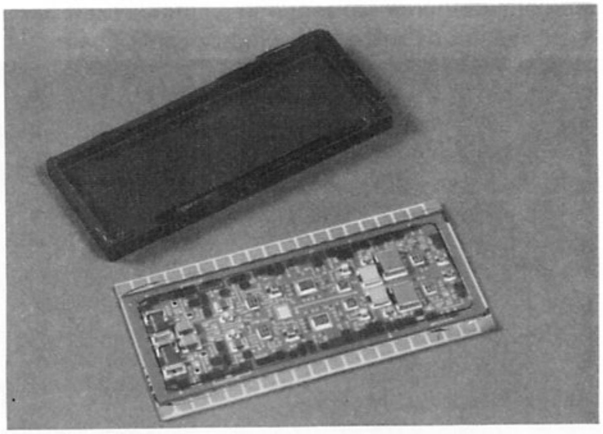

*Fig. 24. Photograph of Vendor A commercial hybrid (as de-capped and after bond pulling)*

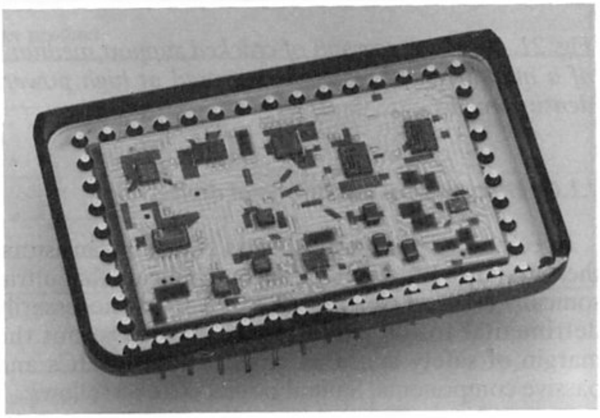

*Fig. 25. Photo of Vendor B commercial hybrid (as de-capped and after bond pulling)*

**Table 5**

**Details of hybrid test vehicles, exposures and examination intervals**

| Board designation | Gold paste type | Gold wire type | No. of boards | Total exposure time (min) | Examination intervals for electrical measurements (min) | Comments |
|---|---|---|---|---|---|---|
| A | 1 | 1 | 6 | 440 | 0, 1, 2, 3, 5, 10, 20, 30, 50, 100, 200, 320, 440 | Power density:11W/litre<br>Solvent: CFC |
| D | 1 | 2 | 11 | 440 | 0, 1, 2, 3, 5, 10, 20, 30, 50, 100, 200, 320, 440 | Gold paste 1: ESL 8836<br>Gold paste 2: ESL 8884 |
| G | 2 | 1 | 5 | 440 | 0, 1, 2, 3, 5, 10, 20, 30, 50, 100, 200, 320, 440 | Gold wire 1: Dr Müller |
| J | 2 | 2 | 13 | 440 | 0, 1, 2, 3, 5, 10, 20, 30, 50, 100, 200, 320, 440 | Gold wire 2: Polyfil |

| Hybrid type | Number of hybrids | Total exposure time after which bond strengths measured |
|---|---|---|
| Metal packaged. Vendor A, type 1 | 4 | 0, 1, 60, 480 min |
| Metal packaged. Vendor A, type 2 | 4 | 0, 8, 18, 168 h |
| Ceramic packaged. Vendor B | 4 | 0, 5, 10, 100 min |

had occurred, confirmed by subsequent examination of all 18 bonds.

(ii) After mechanically opening the test packages, all devices were inspected visually. Some bonds around the periphery of the tiles had suffered mechanical damage, either during lid-sealing operations (that is, glue exuded onto bonds) or during de-lidding. These bonds were discounted for analyses of bond strength distributions.

(iii) To ascertain whether any complete breaks had occurred (in test vehicles or commercial product), and to eliminate time-consuming superfluous bond strength measurement, all device bonds were gently blown with a stream of dry nitrogen. Broken bonds were slightly displaced from their original bonding site.

(iv) Broken/damaged bonds were inspected using scanning electron microscopy to determine the mode of failure.

(v) The strengths of all unbroken bonds were measured using the technique described elsewhere(1,8,9).

### 4.2.4. *Results on hybrids*

*Test vehicles 1*

The initial results indicated that the test vehicles exhibited a high sensitivity to ultrasonic damage. In consequence, the vast majority of the subsequent results were obtained using standard power density exposure (that is, 11 W/litre). The results of the electrical measurements(7) are summarized in figs. 26 and 27. It is clear that, whilst the responses of the four test pieces over the longest time periods were somewhat similar, they were different over the shortest times (corresponding to those used in practical PCB cleaning). These rates of failure are high compared with those experienced with similar gold stitch bonds in cavity packages. However, there are major differences regarding package styles and effective substrates.

The different behaviours demonstrate a dependence on the wire/ink combination; the softer wire initially provides better bonding, with a survival rate

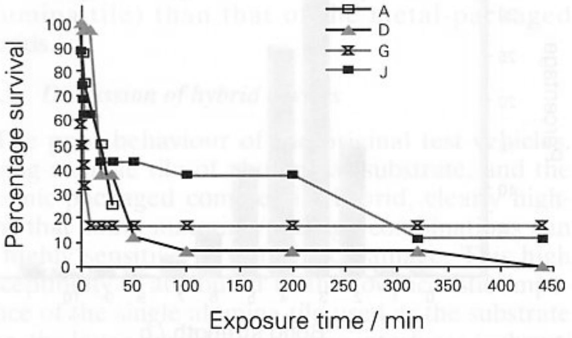

*Fig. 26. Percentage survival as a function of exposure time in CFC for hybrid test pieces*

~ 5 times that of the harder wire, at least over the first 10 min exposure. This is ascribed to both its higher ability to absorb cyclic strain (until sufficient work-hardening has occurred) and its higher ability to deform sympathetically with the substrate. Once the softer wire has become work-hardened, the differences between the two types of wire are minimal.

Microscopic examination after de-lidding the test pieces at the end of the total exposure indicated that none of the failed bonds had lifted from the gold pads. All test pieces displayed breaks at the heels of the bonds, consistent with fatigue as the cause of failure.

Subsequent bond strength measurements indicated that the distribution for virgin test pieces was similar to that obtained for their IC counterparts; the bonds as formed were strong, having average values of ~ 3 g. A composite distribution for the virgin test pieces is presented in fig. 28. After exposure, the strength distributions of the remaining 'good' bonds on all test pieces were similar to those of the virgin test vehicles, again displaying an average value of ~ 3 g.

At this stage, two parameters had been generated for each test vehicle (that is, the number of failed bonds, and the strength distribution of the bonds intact after the full 440 min exposure). These data indicated a high sensitivity of this test vehicle to ultrasonic agitation – a fact that was somewhat surprising in view of the encouraging results on ICs etc. Consideration was therefore given to the amount of energy actually being transferred from the cleaning tank to the gold bonds, especially in relation to that being transferred in typical ICs etc. Emphasis was placed on the probable energy losses through the particular combination of materials and construction used in this test vehicle.

The main conclusion from these considerations$^{(7)}$ was that, as compared with other package constructions, in this test piece a large proportion (~ 94%) of the acoustic energy was being transferred to the bonds, that is, the materials and interfaces were providing only a minor attenuating effect and good acoustic coupling. This was not too surprising since the test piece had been specifically designed to study the apparent high sensitivity of some commercial products.

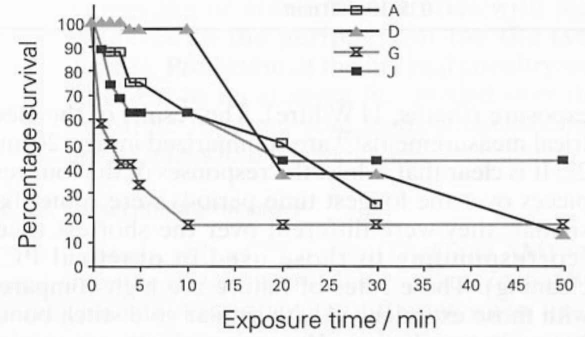

*Fig. 27. Percentage survival as a function of exposure time in CFC for hybrid test pieces*

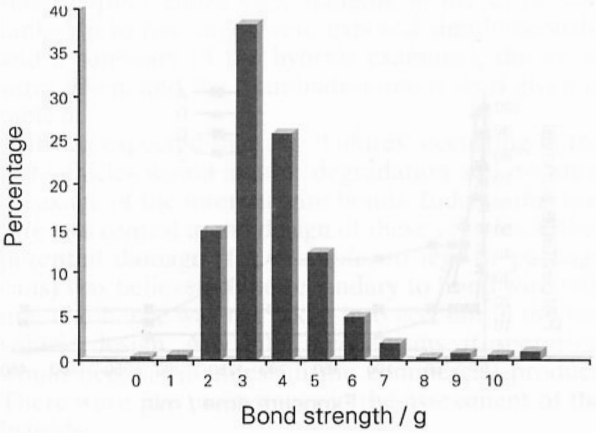

*Fig. 28. Bond strength histogram of virgin hybrid test pieces*

*Test vehicles 2*

In order to test this hypothesis, further test vehicles were modified by adding a second alumina substrate using Araldite under the original substrates, and on another test piece, a third alumina substrate was added. In this way, not only was the actual thickness of the effective substrates much greater, but also the number of interfaces (at which acoustic energy might be lost) was increased. Indeed, the amount of acoustic energy transmitted$^{(7)}$ to the bonds was now <0.1% (doubled substrates) and <0.02% (tripled substrates). These modified test vehicles were then subjected to ultrasonic exposure and, again, the number of failures and the strength distribution of the surviving bonds ascertained.

The beneficial effect of decreasing the effective acoustic coupling is dramatically illustrated in figs. 29 and 30. The results are markedly better than those obtained for the single substrates (compare figs. 26 and 27).

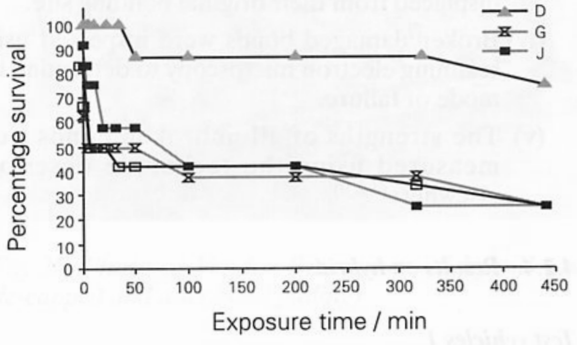

*Fig. 29. Percentage survival as a function of exposure time in CFC for hybrid test pieces having doubled substrates*

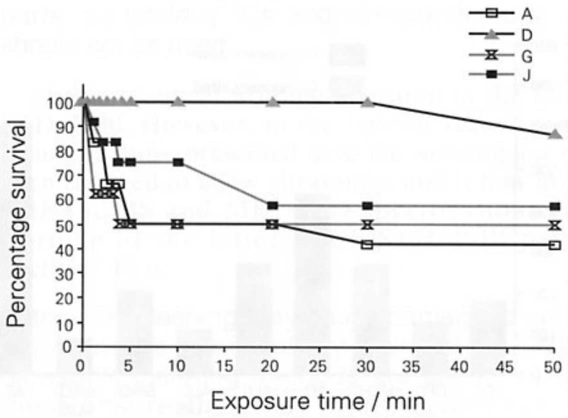

*Fig. 30. Expanded version of fig. 29 showing the first 50 min of the exposure time*

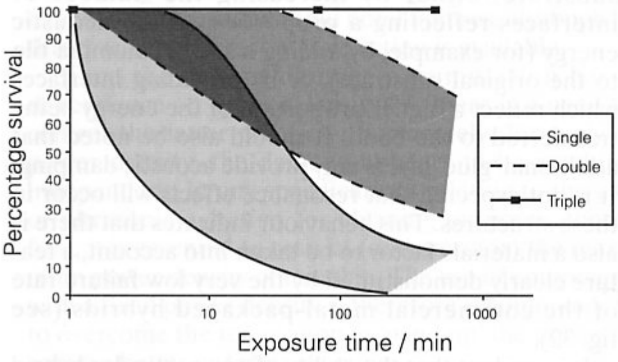

*Fig. 31. Percentage survival as a function of exposure time in CFC for hybrid test pieces having single, doubled and trebled substrates (showing spread of values)*

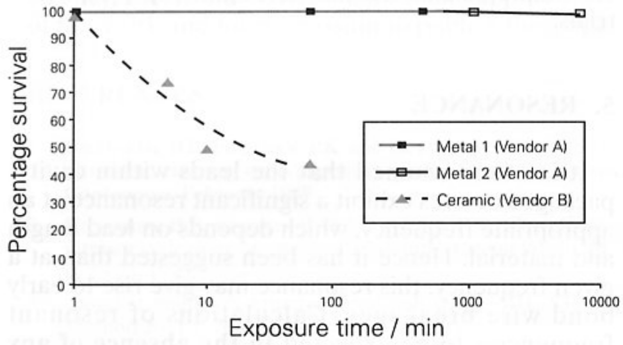

*Fig. 32. Percentage survival as a function of exposure time in CFC for commercial hybrids*

This improved performance was further enhanced when a third substrate was added. In this case, electrical measurements indicated that there were no failures after the full 440 min exposure (compared with an average of 25% failures for the 'doubled' substrate and virtually 100% failure for the single substrate test pieces). A clear demonstration of the markedly different performance of the three types of test vehicle is presented in fig. 31, showing the spread of values for each type.

The main conclusions drawn from these studies on test vehicles are as follows.

(i) Certain combinations of materials and substrates can transfer large proportions of the energy delivered to the cleaning tank to the bonds, and hence impart an apparently high sensitivity to damage resulting in many failed bonds.

(ii) This sensitivity can be drastically reduced by simple modification of the materials/substrates combination, by altering the acoustic impedance of the effective substrate.

(iii) This apparent variable sensitivity of the bonds to ultrasonic agitation, depending on the substrate materials/construction, may well explain the confusing and conflicting reports from the field.

***Commercial product***

The complexity of the commercial product inhibited easy access for electrical evaluation of bond integrity in unopened packages. In consequence, resort was made to bond strength determinations of all the bonds on opening the packages after exposure.

Eight metal-packaged devices (Vendor A) were exposed for up to 126 h and the final bond strengths clearly demonstrated the very low sensitivity of this particular device/package to ultrasonic damage (see fig. 32). No failures (defined as zero bond strength) were encountered for continuous exposure of eight hours, and only three (out of <200) failures occurred after 126 h. By contrast, when four ceramic-packaged hybrids (Vendor B) were exposed for up to 100 min, many bond failures occurred (see fig. 32) clearly demonstrating the higher sensitivity of this product (alumina tile) than that of the metal-packaged hybrids.

### *4.2.5. Discussion of hybrid devices*

The poor behaviour of the original test vehicles, having a single tile of alumina as substrate, and the ceramic-packaged commercial hybrid, clearly highlight that some materials/package combinations can be highly sensitive to ultrasonic damage. This high susceptibility is attributed to the low acoustic impedance of the single alumina tile used as the substrate base, the latter providing only two interfaces (solvent/alumina; alumina/ink) for attenuation of the energy transferred from the tank to the bond. If commercial hybrids have this type of construction, they will exhibit a high sensitivity to ultrasonic damage.

This susceptibility can be minimized, however, by increasing the acoustic impedance of the effective substrate, either by increasing the number of interfaces reflecting a proportion of the acoustic energy (for example, by adding a second alumina tile to the original substrate), or by providing interfaces which reflect a higher proportion of the energy being transferred to the bond. It should also be noted that additional 'glue' layers may provide acoustic damping. It is not expected that resonance effects will occur in these structures. This behaviour indicates that there is also a materials factor to be taken into account, a feature clearly demonstrated by the very low failure rate of the commercial metal-packaged hybrids (see fig. 32).

It is evident that the ability of any particular hybrid to withstand ultrasonic agitation is critically dependent on the design of the particular materials/package combination. Hence careful consideration must be given to the use of hybrids which may be subjected to ultrasonically-assisted cleaning.

If a particular hybrid is to be used in this way simple guidelines need to be generated to assess its sensitivity to damage. Such guidelines can be generated(7) either via simple calculations, or through simple exposure trials.

## 5. RESONANCE

It is often assumed that the leads within cavity-packaged devices exhibit a significant resonance at an appropriate frequency, which depends on lead length and material. Hence it has been suggested that, at a given frequency, this resonance may give rise to early bond wire breakages. Calculations of resonant frequencies to be expected **in the absence of any damping** have been carried out(5,10,11) by a number of workers (including the authors) based on vibrating beam theory. These calculations indicate that for both Al and Au wires (diameter 30 μm) the resonant frequency is <10 kHz for lead lengths of approximately 3 mm, the latter being the maximum length encountered in the IC packages used in this study.

Attempts were made to observe resonance occurring in bond wires of this length in 4116 and 4001-type devices using a vibration table driven at variable frequency (up to 10 kHz) and constant amplitude. The device leads were viewed in a microscope using stroboscopic illumination whose frequency was set slightly different from that of the table such that the vibrational amplitude could be observed. No resonance was detected, the amplitude of vibration being essentially constant over the sweep frequency range. An alternative method of observing resonance using a mechanical impulse technique was also employed, in which an RF signal was applied to the bond wire and the capacitatively coupled signal from the metal package lid was monitored for amplitude modulation during (and following) each mechanical impulse. The resulting signal was of short duration and showed no sign of resonance (that is, the logarithmic decrement was significantly shorter than the period of vibration of the wire).

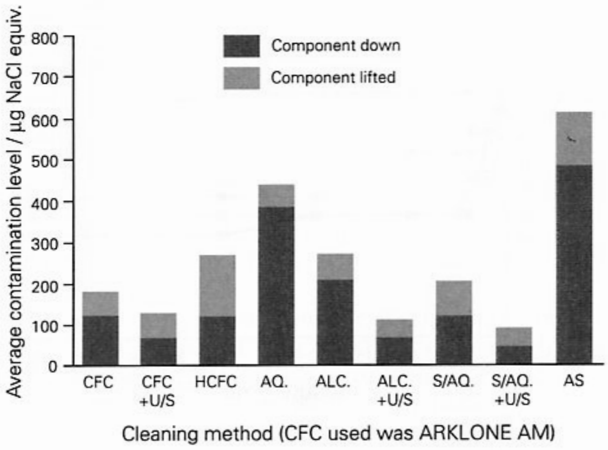

*Fig. 33. Typical comparative data for one cleaning regime from the UK collaborative programme (reference 13)*

## 6. CLEANING EFFICIENCY

In view of the promising results obtained with all three solvents with respect to damage accumulation, it was of interest to investigate the levels of enhanced cleaning efficiencies brought about by ultrasonic agitation. Data demonstrating the cleaning performances of a range of cleaning solvents are readily available in the literature, but until recently there were few data on a truly comparative basis. An extensive range of such data has now become available through a UK collaborative programme(12) and many of the results have been discussed elsewhere(13). A typical set of results is presented in fig. 33 in which the efficacy of the various cleaning options (for a particular set of soldering conditions) can be readily compared. In all cases the levels of cleanliness achieved compared well with those using CFCs, and were within those required by even the most stringent MIL specification. The added advantage of using ultrasonic agitation is clearly demonstrated, and support the earlier findings(1) that under standard power density conditions cleaning was complete within two minutes even for stand-off heights as small as 25 μm.

The important point is that the power density/time combinations required to achieve good cleaning are far removed from those required to produce any component damage.

## 7. STATUS OF STANDARDS

In certain sections of the industry (for example, consumer, telecommunications) the use of ultrasonic agitation is not an issue in the relevant standards, and it has been widely used without deleterious effects for several decades. However, until recently, ultrasonic cleaning had not been allowed by the American military, as evidenced by the following declaration (from MIL-STD-P28809, Section 6.7):

'Ultrasonic cleaning may damage certain component parts, particularly ICs and semiconductors, and should not be used'.

Almost identical wording appeared in the DOD-STD-2000. However, in the light of recent results including those presented here the wording has now been changed to allow ultrasonics, and is now in line with the BS and MIL-STD specifications. The wording of the latter (DEF-STD-0010 part 6, Section 7/F) is:

'Ultrasonic cleaning may cause damage to certain components, particularly transistors. When ultrasonic cleaning methods are used, the user must ensure that they will not damage the components to be cleaned'.

As more experience is gathered with ultrasonically-assisted cleaning in military products, it is expected that the wording will be relaxed even further. As part of the move to gather this information in America, IPC is amending its cleaning handbook to include a chapter on ultrasonic cleaning. It will contain a comprehensive list of those components world-wide that have been ultrasonically stressed, and a standard protocol for evaluating the sensitivity of those that have not.

## 8. GENERAL CONCLUSIONS

The results of this work are very encouraging for users of PCBs in that, if ultrasonic agitation is employed in the cleaning regime, there is a large margin of safety before any damage to a large range of components (ICs, discrete devices, passives etc.) is incurred. This safety margin for CFCs is shown schematically in fig. 18, but the results obtained with aqueous and semi-aqueous solvents indicate that this schematic can be applied more widely. Although the results presented here relate strictly only to the range of components studied, US data(5) obtained on other components (selected on the basis of their sensitivity to resonance effects) suggest that the benign nature of the ultrasonic agitation is of general applicability. If failures do occur during normal ultrasonic exposure during cleaning, then the failure mode is always fatigue, usually at the heels of the bond wires. However, in these cases, the original quality of the components is usually doubtful, and the ultrasonic exposure is simply highlighting this poor quality.

There are, however, some components which do exhibit a sensitivity to the use of ultrasonics. But QCDs and hybrids, often believed to be particularly susceptible, can be used, providing certain guidelines are observed. In QCDs, for example, the margin of safety is not as large as that for ICs and passives. However, once manufacturing defects have been screened out, they will withstand ultrasonic exposure without deleterious effects for periods several times those used for cleaning PCBs.

In the case of hybrids the design of the package is critical in determining its susceptibility to ultrasonic damage and simple guidelines need to be followed to assess the sensitivity of a particular package. Whilst some designs exhibit the same large margins of safety as ICs, others result in rapid bond failures, although in this case simple preventative action is available.

Since the rate of damage accumulation has a dependence on (power density)$^{6.3}$, there is a need to control the latter precisely. Fortunately, for a given power density, the damage appears to be machine independent. In any specifications relating to the use of ultrasonic agitation for cleaning purposes, therefore, it is essential to restrict (and monitor) the maximum power density obtainable. The use of equipment with a fixed power density is therefore recommended, to overcome the temptation to 'wind up' the power to achieve better or faster cleaning.

These results have already been instrumental in achieving a re-working of relevant cleaning standards (BS; MIL-STD; DoD 2000) to allow qualified ultrasonic assistance.

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